UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/548,469	04/13/2000	Balaram Sinharoy	AT9-99-129	7436

7590 11/05/2004

EXAMINER
LI, AIMEE J

Kelly K Kordzik
Winstead Sechrest & Minick P C
P O Box 50784
Dallas, TX 75201

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 11/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/548,469	SINHAROY ET AL.	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14,39 and 40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14,39 and 40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In view of the Appeal Brief filed on 13 August 2004, PROSECUTION IS HEREBY REOPENED. A new grounds of rejection is set forth below.

2. To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

3. If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

4. Claims 1-14 and 39-40 have been considered.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 39 and 40 are rejected under 35 U.S.C. 102(b) as being taught by Hennessy's Computer Architecture: A Quantitative Approach Second Edition ©1996 (herein referred to as Hennessy).

7. Referring to claim 39, Hennessy has taught a data processing system for predicting whether a conditional branch instruction will be taken or not taken (Hennessy page 271, paragraph 4), the data processing system comprising the program steps of:

a. Determining if the conditional branch instruction is positioned at a specified address in a sequence of instructions being executed (Hennessy page 273, paragraph 2 and Figure 4.22; page 274, paragraph 1; and Figure 4.23). In regards to Hennessy, the PCs, or Program Counter, contains the address of the current instruction being executed and the address of the branch instruction address currently being pointed to in the branch-target buffer. For a definition of PC, please see Rosenberg's Dictionary of Computers, Information Processing & Telecommunications Second Edition ©1987.

b. Predicting whether the conditional branch instruction will be taken or not taken as a function of the position of the specified address (Hennessy page 273, paragraph 2 and Figure 4.22; page 274, paragraph 1; and Figure 4.23).

8. Referring to claim 40, Hennessy has taught wherein the predicting program step will predict taken if the specified address is a multiple of specified number N (Hennessy page 273, paragraph 2 and Figure 4.22; page 274, paragraph 1; and Figure 4.23). In regards to Hennessy, every address is a multiple of itself. For example, if the branch instruction is at specified address 20, then the address is a multiple of a specified number 20.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1-14 and 39-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Henry et al., U.S. Patent Number 6,550,004 (herein referred to as Henry) in view of Tanenbaum's Structured Computer Organization Second Edition ©1984.

11. Referring to claim 1, Henry has taught a method for predicting a result of a conditional branch instruction, comprising the steps of:

a. Determining if a specified condition register field is used to store a branch condition of the conditional branch instruction (Henry column 7, lines 36-38 and column 9, lines 31-44); and

b. Providing a branch prediction of the conditional branch instruction as a function of the determination if the specified condition register field is used to store the branch condition of the conditional branch instruction (Henry Abstract, lines 13-14; column 4, lines 49-52; column 5, lines 8-12 and 35-38; column 9, lines 31-44; and Figure 2).

12. Henry has not explicitly taught the branch prediction is done by software. However, Henry has taught branch prediction in hardware (Henry Abstract, lines 13-14; column 4, lines 49-52; column 5, lines 8-12 and 35-38; column 9, lines 31-44; and Figure 2). Tanenbaum has taught that "Hardware and software are logically equivalent...any instruction executed by the hardware can also be simulated in software (Tanenbaum page 11)." A person of ordinary skill in the art at the time the invention was made would have recognized that whether the branch prediction is done in software or hardware, it does not matter since they are logically equivalent.

The branch prediction method taught in Henry can be done in both hardware and software, and it is more a design decision whether to implement the method in hardware or software (Tanenbaum page 11). The decision to implement the method in software or hardware is dependent on which is more optimal in regards to factors such as cost, speed, and reliability (Tanenbaum page 11). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the software taught in Tanenbaum in the device of Henry.

13. Referring to claim 8, Henry has taught a processor comprising:

a. An instruction fetch unit for fetching a conditional branch instruction (Henry column 6, lines 33-50 and Figure 1);

b. Circuitry for determining if a specified condition register field is used to store a branch condition of the conditional branch instruction (Henry column 7, lines 36-38 and column 9, lines 31-44); and

c. Circuitry for providing a branch prediction of the conditional branch instruction as a function of the determination if the specified condition register field is used to store the branch condition of the conditional branch instruction (Henry Abstract, lines 13-14; column 4, lines 49-52; column 5, lines 8-12 and 35-38; column 9, lines 31-44; and Figure 2).

14. Henry has not explicitly taught the branch prediction is done by software. However, Henry has taught branch prediction in hardware (Henry Abstract, lines 13-14; column 4, lines 49-52; column 5, lines 8-12 and 35-38; column 9, lines 31-44; and Figure 2). Tanenbaum has taught that "Hardware and software are logically equivalent...any instruction executed by the hardware can also be simulated in software (Tanenbaum page 11)." A person of ordinary skill in

the art at the time the invention was made would have recognized that whether the branch prediction is done in software or hardware, it does not matter since they are logically equivalent. The branch prediction method taught in Henry can be done in both hardware and software, and it is more a design decision whether to implement the method in hardware or software (Tanenbaum page 11). The decision to implement the method in software or hardware is dependent on which is more optimal in regards to factors such as cost, speed, and reliability (Tanenbaum page 11). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the software taught in Tanenbaum in the device of Henry.

15. Referring to claims 2 and 9, Henry has taught wherein the software branch prediction predicts that the conditional branch instruction will be taken if the specified condition register field is used to store the branch condition of the conditional branch instruction (Henry Abstract, lines 13-14; column 4, lines 49-52; column 5, lines 8-12 and 35-38; column 7, lines 36-38; column 9, lines 31-44; and Figure 2).

16. Referring to claims 3 and 10, Henry has taught wherein the software branch prediction predicts that the conditional branch instruction will be not taken if the specified condition register field is not used to store the branch condition of the conditional branch instruction (Henry Abstract, lines 13-14; column 4, lines 49-52; column 5, lines 8-12 and 35-38; column 7, lines 36-38; column 9, lines 31-44; and Figure 2).

17. Referring to claims 4 and 11, Henry has taught wherein the software branch prediction predicts that the conditional branch instruction will be not taken if the specified condition register field is used to store the branch condition of the conditional branch instruction (Henry

Abstract, lines 13-14; column 4, lines 49-52; column 5, lines 8-12 and 35-38; column 7, lines 36-38; column 9, lines 31-44; and Figure 2).

18. Referring to claims 5 and 12, Henry has taught wherein the software branch prediction predicts that the conditional branch instruction will be taken if the specified condition register field is not used to store the branch condition of the conditional branch instruction (Henry Abstract, lines 13-14; column 4, lines 49-52; column 5, lines 8-12 and 35-38; column 7, lines 36-38; column 9, lines 31-44; and Figure 2).

19. Referring to claims 6 and 13, Henry has taught wherein the specified condition register field is N, where N is an integer (Henry column 7, lines 36-38 and column 9, lines 31-44).

20. Referring to claims 7 and 14, Henry has taught wherein the specified condition register field is a multiple of N (Henry column 7, lines 36-38 and column 9, lines 31-44). In regards to Henry, the field is located anywhere within the condition register, as long as the particular field exists, the prediction is based on this field.

Response to Arguments

21. Applicant's arguments regarding claims 1-14 filed 11 August 2004 have been fully considered but they are found partially persuasive. Specifically, the argument regarding no mention of software branch prediction has been found persuasive and the rejection has been changed to the above to correct this distinction. However, the argument

> ...the Examiner must provide extrinsic evidence that must make clear that a register containing fields where each field may represent a particular flag and where the bit(s) in each field may represent a state of a particular flag discloses

providing a prediction if a condition register field is used to store a branch condition (Applicant's Appeal Brief page 6)...

22. has not been found persuasive. The Examiner provided copies of sections from the Intel Pentium® Processor Family Developer's Manual Volume 3: Architecture and Programming Manual (herein referred to as Intel) regarding the conditional jump test types referred to in Henry. Intel is incorporated by reference in Henry on column 9, lines 40-45. The first Intel section was provided with the original office action dated 03 March 2003 and describes the Flags register. As shown in Figure 3-9 and Table 3-2 on page 3-14, the flags register, named EFLAGS, contains an overflow flag (OF), sign flag (SF), zero flag (ZF), and carry flag (CF). Each of these flags are status flags produced by arithmetic instructions and conditional jumps and subroutine calls respond to these flags (Intel page 3-14 "...the EFLAGS register report the kind of result produced from the execution of arithmetic instructions...Conditional jumps...allow a program to sense the state of the status flags and respond to them."). The Examiner provided another section of Intel with the Final Rejection dated 05 May 2004 describing the conditional jump instructions referred to in Henry on column 9, lines 31-45. As shown on page 4-26 in Table 4-3 and pages D-1 to D-2 in Appendix D.1, Intel has various conditional jump instructions that rely on flag states. The flags referred to in the flag states are the flag fields found in Intel's EFLAGS register taught in Figure 3-9 and Table 3-2. Henry teaches in column 9, lines 31-45 that his branch predictor receives three inputs to predict the outcome of conditional branch instructions. One of the inputs is a conditional branch instruction test type, which includes the x86 conditional jump instruction (JCC) text types, particularly the test types found on pages D-1 and D-2 of Intel, whose entirety is incorporated by reference.

Conclusion

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

24. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

25. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
22 October 2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100